

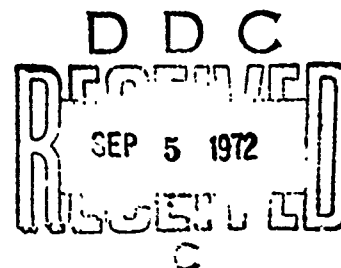
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## ELECTRICAL OVERSTRESS FAILURES IN SILICON DEVICES

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<p>Experimental evidence gathered from overstressing test patterns is presented to substantiate a mechanism proposed by the author for surface overstress failures (surface zaps). The mechanism involves field enhanced migration of liquid along a line determined by both crystal and electric fields. Migration is initiated by field enhanced breakdown from a defect or precipitate in the silicon which leads to current filament formation and a rise in temperature above the eutectic for Al-Si or Au-Si. It is demonstrated that with titanium contacts, surface shorts are eliminated. Graphs are given which show the relationship between breakdown voltage and electrode spacing and between maximum power dissipation and electrode spacing for aluminum contacts to 5 ohm-cm n-type and 0.5 ohm-cm p-type silicon. Oxidation temperature is identified as a factor which affects zap sensitivity as well. Thus, this paper shows the effects of material combinations, electrode spacing, oxidation temperature and alloying temperature on zap susceptibility in planar devices.</p> <p>Details of illustrations in this document may be better studied on microfiche</p>			

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**ELECTRICAL OVERSTRESS FAILURES IN SILICON DEVICES**

**Clyde H. Lane**

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## FOREWORD

The author is indebted to various members of the Solid State Applications Section, Reliability Branch, RADC, for contributions to the processing of the test patterns; particularly to Thomas Walsh and Janson Engler for the photolithography and testing. Timely discussions with and some testing by members of the Reliability Physics Section are also acknowledged, particularly the contributions of Jack S. Smith who often played the devil's advocate and is involved in short pulse overstress testing. This in-house work was sponsored by Job Order No.: 55190000, "Reliability and Maintainability Techniques for Electronics." It was presented at the Technical Conference on Recent Advances in Electronic, Optical and Magnetic Materials, 20 August - 1 September 1971, San Francisco, California. The conference was sponsored by the Metallurgical Society of AIME.

The report has been reviewed by the Information Office, RADC, and is releasable to the National Technical Information Service.

This technical report has been reviewed and is approved.

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### ABSTRACT

Experimental evidence gathered from overstressing test patterns is presented to substantiate a mechanism proposed by the author for surface overstress failures (surface zaps). The mechanism involves field enhanced migration of liquid along a line determined by both crystal and electric fields. Migration is initiated by field enhanced breakdown from a defect or precipitate in the silicon which leads to current filament formation and a rise in temperature above the eutectic for Al-Si or Au-Si. It is demonstrated that with titanium contacts, surface shorts are eliminated. Graphs are given which show the relationship between breakdown voltage and electrode spacing and between maximum power dissipation and electrode spacing for aluminum contacts to 5 ohm-cm n-type and 0.5 ohm-cm p-type silicon. Oxidation temperature is identified as a factor which affects zap sensitivity as well. Thus, this report shows the effects of material combinations, electrode spacing, oxidation temperature and alloying temperature on zap susceptibility in planar devices.

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## INTRODUCTION

For several years, electrical overstress (EOS) failures, which occur when stated device electrical limits have been exceeded, have been seen in silicon devices and integrated circuits. Generally, the problem appears to be one of human factors or design compatibility combined with a reduced stress tolerance for surface shorts. Several papers (1, 2, 3) have addressed types of effects resulting from EOS and the human factors and handling problems associated with them. The concern of this paper is with the reliability aspects, specifically, what occurs during EOS, and what can be done in fabrication and materials usage to provide the greatest tolerance to over-stress? We know that some devices are destroyed completely through shorted junctions, usually surface shorts, or through burned out metallization, often at contact steps. In other instances, transistor beta's are permanently degraded but the device or circuit still operates. It would be desirable if the device and reliability engineer could solve the problem completely from the device fabrication standpoint, thereby clarifying the remaining problems of the design or compatibility engineer involved in assessing and controlling sources of electrical transients in electronic equipment.

In this study, the approach taken to accomplish that end was to attempt to explain the nature and cause of surface zaps. Since aluminum seemed to have moved from one contact to another, emitter-base, base-collector, etc. beneath the silicon dioxide

passivation layer in the failures seen, study of the phenomenon was a natural extension of the author's work on aluminum migration at the silicon - silicon dioxide interface<sup>(4)</sup>. In fact, that previous work immediately suggested the cause and a cure for the surface zap problem (Electrical Overstress). The effort expended on this program was to verify the author's hypothesis and prove that surface zaps may be eliminated. When this is done, one can concentrate more on metallization burn-out and bulk type junction shorts. Cures for these portions of the EOS problem are defined by material parameters, process induced defects, junction limitations and practical considerations such as metallization thickness.

Before stating the hypothesis and proceeding with discussion of the work, it should be noted that the mechanism of electrical overstress failures very likely depends markedly on the transient pulse width. In this work, the focus is on long pulses. An exact definition of long cannot be given, but generally pulse widths greater than one microsecond will qualify. This is because aluminum may be detected in the zap channel caused by a pulse of that width or larger, as will be shown later in the text on the basis of a 50 microsecond pulse test used to establish the lower limit validity for the results presented. Below one microsecond, there may be a transition to another mechanism as temperatures get higher. From 10 nanoseconds down, it is felt that thermal time constants are too long for appreciable heat dissipation. Thus, temperatures may easily rise to the silicon melting point.

Most EOS failures seen by failure analysis people at RADC (Rome Air Development Center) and by the author, show aluminum in the channel. These failures, which account for 70 percent to 80 percent of the device or circuit failures analyzed by the failure analysis group, are definitely the long pulse type.

The hypothesis mentioned earlier, which will subsequently be substantiated to a great extent, is as follows. Surface zaps in planar silicon devices (those which occur at the silicon surface beneath the passivating oxide) are caused by breakdown and filamentary conduction from defects introduced predominately during oxidation. Temperatures at the tips of the defects, where microplasmas may exist, easily rise to 700°C. At such temperatures, molten silicon - aluminum alloy can have an interface migration velocity of at least  $10^2$  centimeters per second. The migrating liquid alloy follows the breakdown filament or microplasma toward the opposite electrode at accelerating speed. This is the cause of the surface short and the reason for its appearance. This immediately suggests a cure; use a metal like titanium in contact with the silicon. Since titanium has no low temperature eutectic with silicon, hot spot migration will not occur. The temperature in the filament must then rise to the silicon melting point before permanent damage is done.

#### PROCEDURE

Examination of test patterns was considered the best way to

proceed. Use was made of some existing patterns and new ones were designed for special purposes. All patterns are shown in Figure 1. The first pattern tested (Pattern A) was, in fact, a pattern used in the previous study<sup>(4)</sup> of aluminum to silicon alloying. Electrode separations were large on this pattern and there was no oxide passivation on one of the wafers used. Pattern C was designed for another group to study electromigration and metallization burn-out, and was used in this study because it had two convenient sets of contacts of appropriate separation, 30 and 58 microns. Pattern B was designed to show the effect of alloy triangles on zap shorts. The aluminum triangles were produced by a two minute alloy at 600°C. Finally, pattern D was designed to study the effect of contact type (n or p silicon) electrode spacing, oxidation process and type of metallization on EOS shorts. There were no diffusions under the contacts in patterns A, C or D, only in pattern B. Therefore, we are not dealing with diffused diodes in most cases, only with ohmic and Schottky contacts and alloy type diodes.

Contacts were made to the electrodes via tungsten probes connected to the Tektronix 575 curve tracer. Power was applied in one of two ways. Usually power was applied gradually by turning up the voltage with a preset limit resistor in the circuit. In this way, one could follow all the events that lead to breakdown. Voltages and currents were noted at various points of interest as the power was increased. The other method used for some samples was to preset the voltage and limit resistor

to values which would insure failure and apply power by quickly working the toggle switch. This approach was used to provide a number of zaps which resembled field failures. The zaps were then etched and lapped and etched again to find out what the channel consisted of physically. Both 30° and 90° angle laps were examined.

Initially, aluminum metallization on 5 ohm-cm, (111) orientation, n-type silicon was studied using wafers oxidized at 1000°C in steam. These contacts were alloyed to the silicon and appeared to be alloy type p-n junctions. They showed the normal reverse breakdown and second breakdown characteristics of junctions. The general characteristics of zaps were noted on these patterns. Next, aluminum was deposited on both 5 ohm-cm n-type material and 0.5 ohm p-type material. The wafers had been oxidized in steam at 1150°C to an oxide thickness of 6300 angstroms. Alloying was first done at 450°C for 15 minutes in nitrogen. Following measurements of turnover (avalanche) voltage, breakdown (zap) voltage and current at breakdown, four devices were removed from each wafer and sent to another group for shorter, controlled pulse tests. The wafer was then placed back in the alloying furnace at 550°C for 15 minutes. Voltages and currents were again measured for various contact separations.

The next batch of wafers, consisting of two 5 ohm-cm n-type and three 0.5 ohm-cm p-type, was oxidized in steam at 950°C, 200°C lower than the first batch. The oxide thickness was kept the same. A wafer set consisting of one n and one p-type wafer

was aluminized, another set received about 600-700 angstroms of titanium followed by several thousand angstroms of aluminum. On the fifth wafer, p-type, a gold film was sputtered to a thickness of about 2500-3000 angstroms, and the metallization pattern etched. A thin organic film was left on this wafer which later served to provide a thermograph of zaps.

Measurements from the curve tracer are reported as read. They were not corrected for variation from absolute standards and may be off by as much as 20 percent. In addition, the applied voltage is in the form of a rectified sine wave, 240 Hz. As a consequence, actual power dissipation is some fraction of that calculated by simply multiplying maximum voltage at zap by the associated current. The values of voltage, current and power are, therefore, relative and valuable only for comparative purposes. Accurate measurements on shorter pulse zaps have been made with special pulse testing equipment<sup>(5)</sup>. Presently, a complete mathematical model and computer program are being worked on at RADC and should be available within another year. Photographs were taken on the Leitz Ortholux or Orthoplan Metallograph.

#### RESULTS

The first observation following the application of power to electrodes of pattern A was that no surface zaps could be generated. Electrodes in the pattern were simply too far apart, 0.012 inches in the cases under discussion. Nevertheless, interesting information was generated with the pattern. For example, it was noted that migration of aluminum beneath the

$\text{SiO}_2$  passivation layer occurred only from the positive electrode, that is, in the direction of the field. Evidence of this migration is seen in Figure 2. Since migration of this type requires temperature above the eutectic, we know that the joule heating raised the temperature to something above  $577^\circ\text{C}$ . Judging by the appearance of the negative electrode, the temperature there must have been close to  $577^\circ\text{C}$ , but no migration occurred. In another set of patterns, which had no oxide passivation, the aluminum again showed migration from the positive electrode, but the form was that of a pointed finger extending from the electrode in one of the 211 directions, Figure 3. It is likely that the aluminum is following the highest field line allowed by the single crystal constraint on lowest migration energy path. Aluminum protrusions or spikes reached a maximum of 0.003 inches before failure, which occurred through the bulk and not along the surface. The negative electrode turned black due to dissolution of silicon before breakdown, but no metal protrusions were seen from that electrode. Since these contacts were to 5 ohm-cm n-type material, we, in effect, have a forward and a reverse biased diode in series. On one of these electrode sets, the limit resistor and voltage were set to allow spike formation but not bulk breakdown. The toggle switch was then repeatedly exercised. The result was a total of six spikes as seen in Figure 3. When shut off, the spike would not reinitiate but a new spike would form. The points of these spikes were clearly formed by (110) plane boundaries and the spike direction was



perpendicular to the third boundary plane.

Having observed several bulk type overstress failures, as opposed to surface failures, it is very evident that in this case the temperature rises above the silicon melting point. Clear evidence of silicon recrystallization surrounding a bulk zap has been seen. Cracked silicon has been noted in bulk type EOS failure and is occasionally associated with surface zaps.

Pattern C was used to demonstrate that field emission of carriers from alloy triangle points would initiate a surface zap. While these triangles result from considerable overalloying, they do show the effect nicely. Under power, microplasmas observed as points of visible light formed at the vertices of each triangle. As power input increased, the aluminum melted back from the vertex experiencing the highest field. This is seen in Figure 4. A careful look showed that although the aluminum pulled back, the triangular outline remained intact beneath the oxide. This means that a space between the oxide and the silicon, probably a vacuum, exists when the aluminum melts back. Such a point is still a field focal point. When the zaps finally occurred in this sample, the paths clearly went from a vertex of the triangle on the positive side to the vertex of a triangle on the negative side as Figure 5 shows. In this sample, a break or preexisting pinhole in the oxide accidentally provided an excellent photograph, Figure 6, of an incomplete zap path. Note in the lower left-hand corner of the photograph that an arrow of aluminum is pointing toward a negative electrode which

is out of sight. Had this arrow completed its flight, we would have had another zap path. Also, note the aluminum in the zap path emitting from the point of the triangle which had existed at this contact cut.

Next, the effects seen in experiments with pattern B will be described. With these sets of contacts, one again essentially has two alloy diodes back to back with a resistor between them. When power was applied, a normal reverse breakdown was seen, then the device went into second breakdown. In this condition, the metal at the negative side (i.e., the forward biased side) would dissolve silicon and experience grain growth. The contact area would, in fact, turn black. Figure 7 shows the effect. This, of course, is due to joule heating in virtually a steady state situation. Usually, the negative electrode was more severely heated than the positive electrode, yet the zap initiated from the positive side. When the limit resistor was reduced enough, a zap would occur, but not before, even though the device was in second breakdown. By setting a value of voltage and limit resistor which would result in second breakdown, but not a zap, and allowing pulse trains through via the toggle switch, one may follow the sequence of events which transpire at an overstressed contact. To toggle back and forth requires about one-fifth of a second. Figure 8 shows the result of the first pulse train. One sees slight separation at the contact step, some silicon dissolution and aluminum grain growth. Following the second pulse more pronounced aluminum separation is seen as well as

conspicuous grain growth. After the third pulse, Figure 9, the aluminum has completely pulled away from the contact step, there is considerable damage in the contact area and a flashover has occurred adjacent to the initial damage. The flashover did not short the device.

In second breakdown it is known that filaments form which conduct high currents. Evidence for such conduction filaments, in addition to the flashover was seen at both positive and negative electrodes. Figure 10 is a photograph showing traces of conduction filaments. These traces were produced by the high temperature generated by the conduction filament beneath the oxide, which caused aluminum on top of the oxide to melt and recrystallize along the path. There are two paths in this photograph. In spite of the feeling that the zap should initiate where all the damage is being done, ample evidence exists to prove that the zap actually does go from the positive to the negative side regardless of the silicon type. In Figure 11, for example, while extensive damage is seen at the negative side, it is obvious that aluminum has moved from the positive electrode. First, it is wider on that side, and second, the highest temperature for the longest time was experienced above the zap on the positive side as evidenced by the greater aluminum melting (black area) and flow.

To prove that aluminum was actually in the zap channel, the zap region was angle lapped and placed in an aluminum etch. In addition, it was p-stained to see if aluminum had alloyed into

the silicon, changing the n-type to p-type. Figures 12 and 13 give the results. In Figure 12 one sees two paths, a black, hazy, straight path and a serpentine path which appears to contain aluminum. In certain areas the aluminum looks thick. There is no channel beneath the hazy straight path, but a roughly semicircular channel filled with polycrystalline material forms the serpentine path. Aluminum etch readily attacks material in the channel and gives the black region seen in Figure 13. Continued etching removes the white areas entirely. Surprisingly, the p-stained revealed a pronounced p-type area, six microns deep, exactly beneath the hazy path and continuous from it. Diffusion to that depth in the time allowed would require a temperature close to the melting point of silicon, but there is no evidence of damage at the surface to suggest this, and the oxide was not disturbed. The only other satisfactory explanation is alloying from a thin surface layer of Al - Si eutectic. After angle lapping, some chips were mounted for cross sections. Figure 14 shows such a section revealing the hanging drop shape of the zap channel. The black line from which it is hanging is 6000 angstroms of thermally grown silicon dioxide. Over the oxide one can see the aluminum metallization. Another section which was placed in aluminum etch can be seen in Figure 15. This is almost a hemisphere and aluminum has been etched out of the channel as well as from the surface of the chip. Several measurements of the maximum voltage applied before breakdown have average values of 155 and 211 volts for 30 and 58 micron

separations, respectively. Setting x equal to the junction breakdown voltage and y equal to the voltage drop per micron one can calculate the junction breakdown voltage and the field across the remainder of the silicon as follows:

$$\begin{array}{rcl} x + 30y & = & 155 \\ x + 58y & = & 211 \\ \hline 28y & = & 56 \\ y & = & 2 \text{ volts} \\ x & = & 95 \text{ volts} \end{array}$$

Two volts per micron equal a field strength of  $2 \times 10^4$  volts per centimeter. Peak field across the junction is about  $1 \times 10^6$  volts/cm, assuming a depletion region of  $1 \times 10^{-5}$  centimeters. The junction, however, is ill defined and any comparison with theoretical breakdown is of marginal value. More care was taken with Pattern D tests to note voltages and currents at critical points. The first group which was oxidized at 1150°C, alloyed at 450°C, overstressed and then alloyed again at 550°C, showed voltage versus electrode spacing variations depicted in Figure 16. For n-type material there was normal breakdown, microplasma formation and a continued increase in voltage and current until finally the zap occurred. The turnover voltage is the initial breakdown while the breakdown voltage is the voltage recorded when the zap occurred. Curves for n-type material were unaffected by the higher subsequent alloying. Contacts to the p-type material had very different I-V characteristics on the oscillograph display. Figure 17 gives a plot of power dissipation versus electrode spacing for the four combinations of conditions. Apparently there was a lower contact

resistance after the alloying at 550°C for the p-type, allowing a greater current flow. 500°C seems to be required for good ohmic contacts even to relatively low resistivity p-type material. Photographs of the zaps are shown in Figures 18 and 19. Shorts across contacts to n-type material are all similar to Figure 18 regardless of alloying condition. They grow from the positive terminal and are very similar to each other for the same electrodes. On occasion the aluminum arrow does not completely transverse the space between the electrodes. This is seen also in contacts to the p material as Figure 19 shows. Strangely enough, if power is again applied to partially zapped electrodes, a new path will appear, rather than an extension of the old path. Again, the zap direction is positive to negative. Four chips were each hit with a single 50 microsecond pulse to see how damage from the controlled pulse would compare with that generated by the curve tracer. As expected, the same effects were noted in all details. The controlled pulse allowed a calculation of velocity for aluminum migration. The zaps crossed a  $225 \times 10^{-4}$  cm gap in  $50 \times 10^{-6}$  sec; therefore, the velocity for this migration must be at least 450 cm/sec. At this rate, one could short an emitter-base junction, where the junction is 5 microns, or 0.2 mils from the contact, in one microsecond. It is not difficult to believe then that this mechanism is operable into the nanosecond region.

A new group of wafers was oxidized at 950°C in steam and metallized with gold, aluminum or titanium. The wafer having

gold metallization also had a thin organic film on the oxide surface. It was alloyed at 340°C for 2 hours. The turnover and breakdown voltages were the same as for aluminum metallization to 0.5 ohm-cm p-type silicon. Figure 20 shows an incomplete zap involving gold. The same features characterize this failure mechanism as had been observed with aluminum, namely, greater heating on the negative side with obvious plasma formation and zap initiation from the positive side. Voltage was applied again and, as with aluminum, the initial spear did not lengthen but a new spear was generated. There was additional gold migration from the negative side during the second pulse. The extent of gold migration from the negative side exceeded that seen in aluminum contact metallization. The organic film in this case provided a nice thermo-graph seen as a hazy halo surrounding the fold spear. It was noticed that the gold does not take on a triangular shape at the tip as does aluminum, and it may not follow a 211 direction at all, as the aluminum often does. Figure 21 shows a gold protrusion from the positive side. This is the very start of a zap. More power would have pushed that gold out in the form of a spear toward the negative electrode. Gold was removed from the surface for this photograph showing that gold is beneath the silicon dioxide surface. The discolored region is the result of incomplete removal of the overheated thin organic film.

Titanium metallization was alloyed at 550°C for 15 minutes to both n and p-type material. No low temperature alloy forms, however, so no surface zap was expected. No surface zap occurred. The units were submitted to overstress testing prior

to alloying and again following alloying with the same result; only bulk zapping was observed. No shorts were actually detected because the silicon melted, blew out and caused contact to the probes to be lost. Aluminum was deposited over the titanium to protect it during alloying. When aluminum was left on during testing, it would walk around the titanium, contact the silicon and zap in the usual manner. When aluminum was removed, there were no surface shorts. Figure 22 shows the type of failure experienced with titanium contacts. The contacts to p-type material showed more burning and blow-out than the contacts to the n-type material.

Finally, we have a comparison of aluminum alloyed to n and p-type wafers where the oxide was grown at 1150°C and at 950°C. Both sets were alloyed at the same temperature, 550°C, for 15 min. Again all the same characteristics were noted for the lower oxidation temperature wafers. In Figure 23 a partial zap is seen moving in a 211 direction from the positive electrode. More damage is observed at the negative electrode. This set of electrodes did not short. Following the photograph, voltage was again applied. The results are seen in Figure 24. Note that the original zap path has almost disappeared and that a second, continuous zap path started from an aluminum protrusion seen in Figure 23. The second zap turns 60° to complete its journey in a 211 direction. Other things noted in the examination of these zaps were that there were cases where it was impossible to say definitely that aluminum had migrated between the electrodes.



Only a faint hairline remained of the original aluminum path. This is due to a very narrow initial path which subsequently diffused away, or alloyed in because of the high temperature generated. It was also noted that when aluminum (in a zap path) melts back as a result of a second zap nearby, a black hazy line is left. This explains the double paths often seen in earlier work and shown in Figure 12. Perhaps the most important new information revealed by the lower oxidation temperature wafers was that the sensitivity to zap failures is increased by the lower oxidation temperature, particularly for 5 ohm - cm n-type wafers. This may seem surprising at first but the existence of more interface states at the Si-SiO<sub>2</sub> interface<sup>(6)</sup> when the oxide is grown at lower temperatures may explain why the surface zap susceptibility is increased. The graph of Figure 25 compares the zap voltage with electrode separation for aluminum metallization to 5 ohm - cm n-type wafers oxidized at various temperatures.

These results have answered several questions and provided an understanding of how to proceed to remove surface zaps. It would be very desirable now to provide sophisticated follow up experiments to quantify the results and to fix the limits of silicon technology with respect to EOS failures.

#### DISCUSSION AND CONCLUSIONS

The findings of this investigation are:

- (1) Electrical overstress failures in silicon devices are caused by surface shorts, bulk silicon shorts, or open

metallization;

(2) Surface shorts require a metallization such as gold or aluminum which form eutectics below about 800°C.

Titanium contacts for example will not surface zap;

(3) High temperature oxidation provides devices with higher resistance to surface zaps than low temperature oxidation;

(4) In the zap process, a current filament forms which reaches a temperature of 700° to 800°C. This allows rapid alloy migration;

(5) The initial breakdown is a high field breakdown from a point such as a crystallographic defect or an alloy triangle in (111) orientation;

(6) The metal always flows in the direction of the field;

(7) Contact damage is usually greater at the negative contact for the particular contacts involved and micro or mesoplasmas are often seen, first, at outside corners of the contact, and then, along the contact cut. Thermally induced metal migration often occurs from this electrode, but field migration is weak although it appears to occur with gold.

These observations lead one to a mechanism of field breakdown which very early was cited as a cause of surface breakdown as opposed to bulk or theoretical junction breakdown. A 1962 RADC Technical Report<sup>(7)</sup> states that silicon transistors sometimes have their collector junction breakdown voltages lowered when the device is given a sharp rap when under a large

applied bias voltage. Breakdown is a microplasma type. Once the breakdown voltage has been lowered in this way, it remains low until the device is etched, indicating a surface effect. In this report it was also noted that a compressive stress of  $4 \times 10^4$  lbs/in<sup>2</sup> caused a doubling of the current when the device was in reverse bias. Most of the excess current disappeared when the stress was removed. The strain energy density, about  $2.5 \times 10^{-5}$  electron volts/atom is too low for a bulk effect in a perfect crystal. The effect must therefore be a surface effect or a dislocation in the bulk. One other observation was that the breakdown voltage increased as the junction temperature rose from 24°C to 110°C. These effects bear on the surface zap mechanism because the surface is in a stressed condition and junction heating is an intimate part of overstress failures.

In discussing destructive reverse breakdown in a particular type of high voltage silicon junction, Thompson and Wilkinson<sup>(8)</sup> noted that a field breakdown preceded thermal breakdown and made the following observations which fit very well with the results of our experiments:

- (1) Only in the final stage could one consider the characteristic as thermal breakdown;
- (2) The high voltage mode of breakdown occurred at lower voltages for surface breakdown, direct observation of surface breakdown revealed that the initiating mechanism was a field effect, and a mesoplasma was formed in the final stage. Correlation was established between deterioration of the

I-V characteristic and degrees of surface damage;

(3) Surface and bulk breakdown differed only in the magnitude of the leakage current;

(4) Surface breakdown corresponded to a mesoplasma switching on;

(5) Both surface and bulk breakdown in their final stages exhibited thermal breakdown of a known type;

(6) Time of formation of breakdown in p-n junctions is more indicative of an ionization rather than a thermal mechanism.

Hoffman<sup>(9)</sup> in 1964 showed the orientation dependence of breakdown for alloyed silicon rectifiers. He pointed out that hot spots occurred at points where circular junctions coincided with (110) plane intersections. He also noted that during avalanche breakdown, which would preferentially occur from these points, the current would not rise as rapidly as one might expect because of the positive temperature gradient of the avalanche breakdown voltage. Breakdown voltage increases as the temperature rises<sup>(10, 11)</sup>. These facts again argue for the hypothesis stated in the introduction. Finally, the conclusions from an in depth analysis of actual EOS failures indicated that high reverse voltage is more apt to cause open metallization than high current pulses. Open metallization is very often traced to a shorted junction. The metal opens after the junction goes.

The obvious conclusion from the experiments and from the literature is that EOS failures result from field breakdown at structural or chemical defects in the silicon or, if the section

is flawless, from the sharpest point along the junction. Surface zap initiation is similar to bulk except that the field is lower and the thermal breakdown which follows will cause metallization such as gold or aluminum to alloy and follow the field, causing a short. The way is clear then to reduce or eliminate the problem by getting rid of the defects and not allowing a reservoir of aluminum or gold to contact the silicon.

The effect of the oxidation temperature is not entirely clear. One would expect higher interfacial stress but a lower interface state density from the higher growth temperature. It appears that the interface state density should be minimized regardless of the higher stress. Since the effect was pronounced on the 5 ohm - cm n-type wafer, but not on the 0.5 ohm - cm p-type wafers, the conclusion is that the accumulation of the n surface leads to higher filament current for a given voltage and therefore the required temperature to form the molten alloy is reached at a lower applied voltage. In the case of the p-type material, the surface is being depleted and a lower current would flow for a given voltage if higher resistivity material had been used. For 0.5 ohm - cm material, the change is not noticeable. This experiment should be redone to verify the results. At that time, higher resistivity p-type should also be examined.

These experiments have generally confirmed the hypothesis and shown how to avoid surface zaps. Those interested in short pulse failures should again be cautioned however, that the mechanism suggested here may not extrapolate into the region of interest.

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NOTE

The figures for this report are on pages 23 through 36, inclusive.

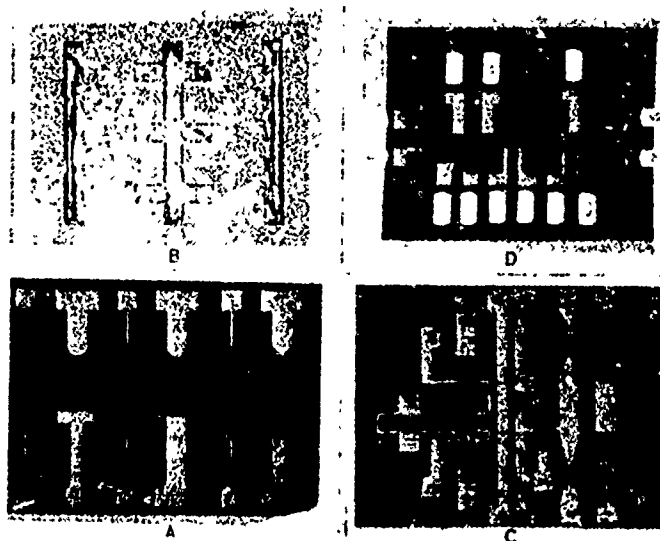


Figure 1

Test Patterns for Zap Studies

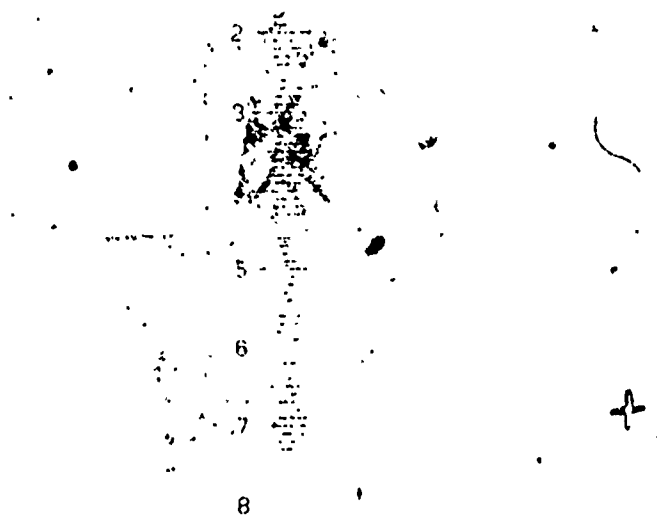


Figure 2

Aluminum Migration at Contact  
Following Application of a Large E Field





Figure 3  
Fingers Extending From a  
Positive Electrode After Pulsing



A



B

Figure 4  
Positive Electrode Before (a) and  
After (b) Application of High Voltage



Figure 5  
Zaps From One Aluminum  
Triangle to Another



Figure 6  
Aluminum Migration Along Zap Path and  
an Incomplete Zap

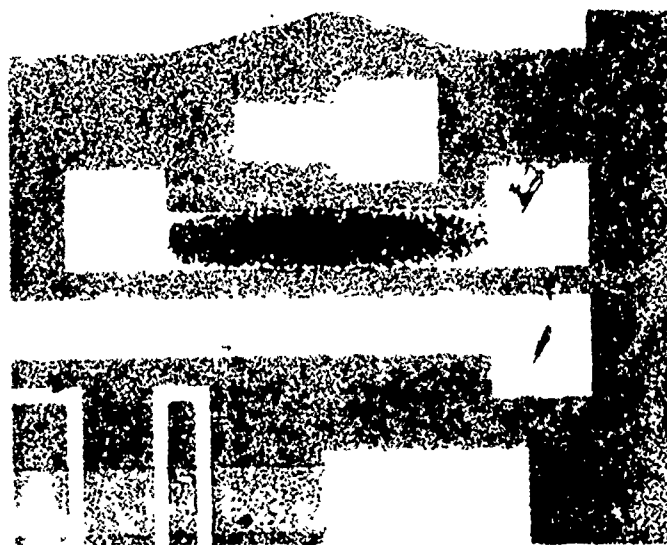


Figure 7  
Grain Growth and Silicon Dissolution  
Due to I<sup>2</sup>R Heating

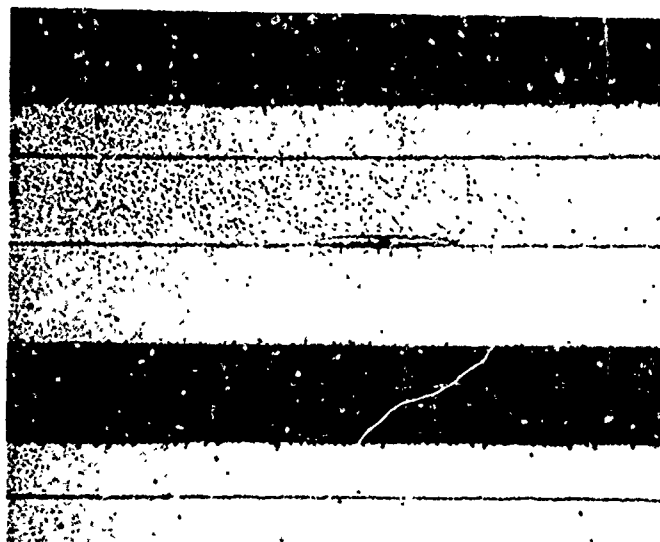


Figure 8  
Start of a Zap



Figure 9  
After Three Pulses, Severe Aluminum  
Degradation and a Flash Over,  
But No Short

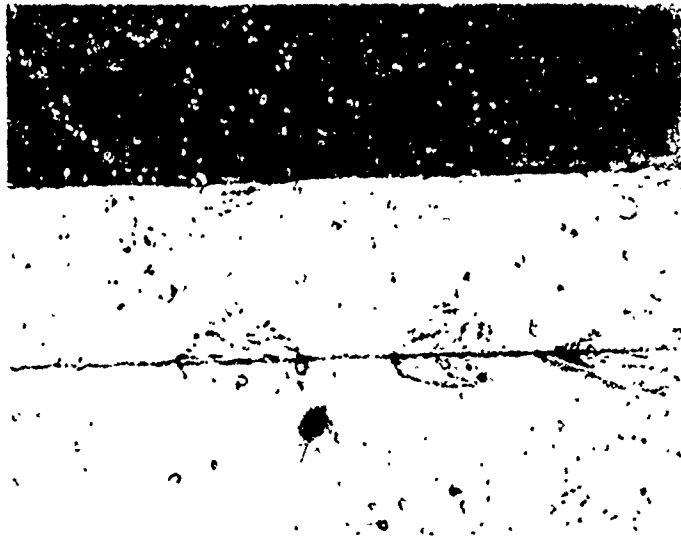


Figure 10  
Evidence of Conduction Filaments  
Beneath the  $\text{SiO}_2$ , Negative Side



Figure 11  
Surface Short; Apparent Propagation,  
Positive to Negative



Figure 12

Double Path in Surface Short

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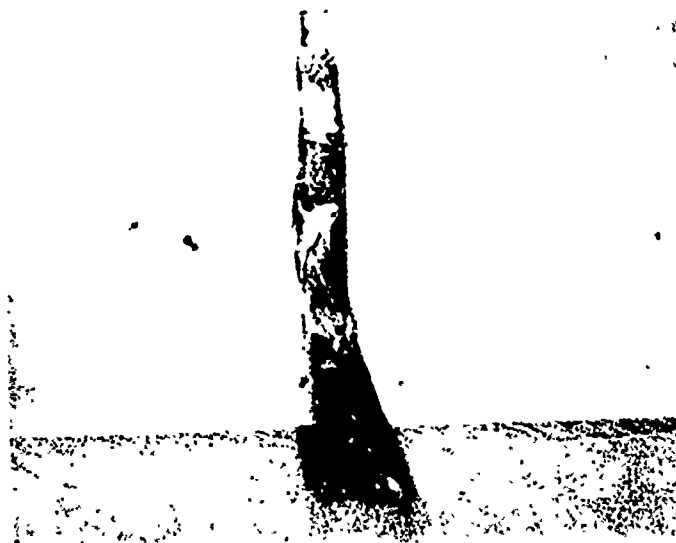


Figure 13

P Stained, Angle Lapped Zap

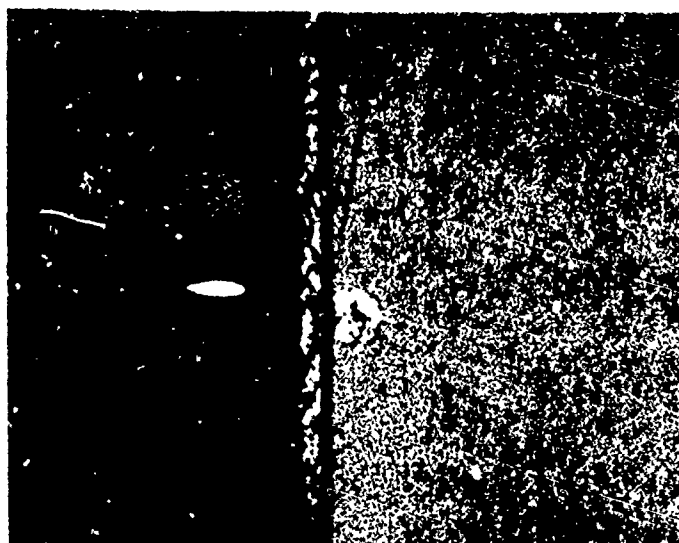


Figure 14

Cross Section of a Zap Channel

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Figure 15

Cross Section of a Zap Channel:  
After Aluminum Etch

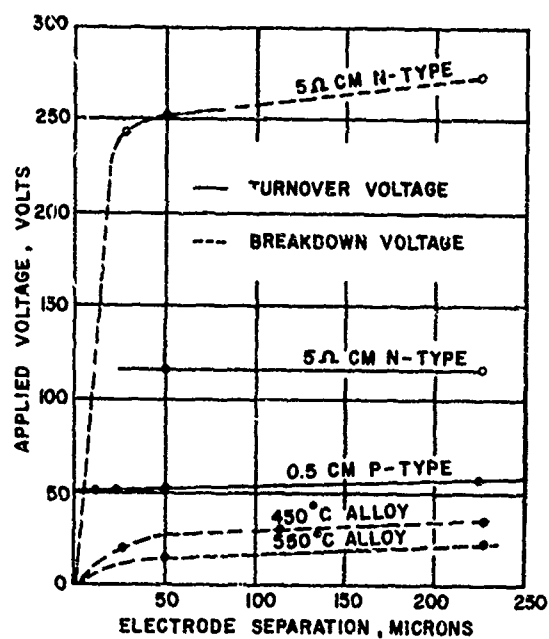


Figure 16  
Variation in Turnover and Breakdown  
Voltages as Function of Electrode  
Separation for Aluminum Contacts

Figure 17  
Variation in Maximum Power Dissipation  
with Electrode Spacing for  
Aluminum Contacts

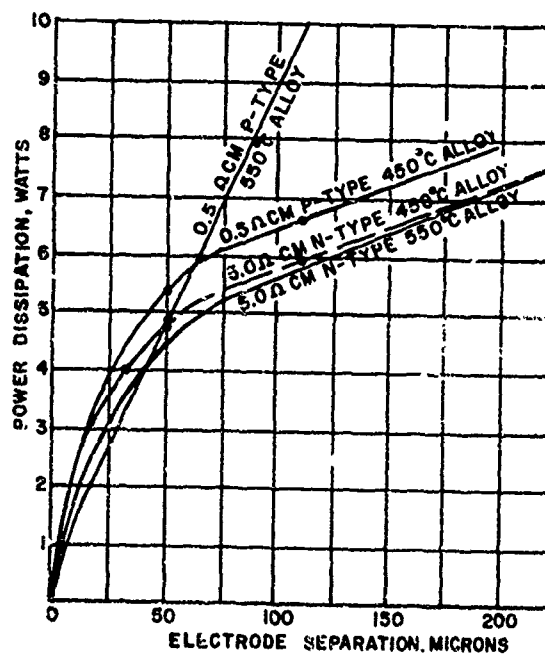






Figure 18  
 Typical Zap for Al to 5 ohm-cm n Type  
 Silicon, 50 Micron Separation

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Figure 19  
 Typical Zap for Al to 0.5 ohm-cm  
 p-Type Silicon, 112 Micron Separation



Figure 20  
Multiple Partial Zap Paths From the  
Positive Electrode and Slow Gold  
Migration from the Negative Electrode

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Figure 21  
Gold Protrusion From the Positive  
Electrode Prior to Zap




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Figure 22  
Cratering in Contacts to  
Silicon Covered with Titanium

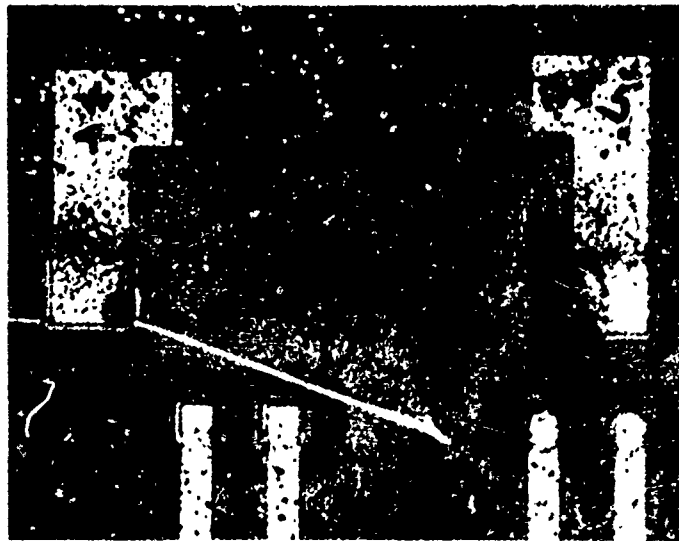


Figure 23  
Partial Zap in 211 Direction  
on 950°C Oxided Wafer


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Figure 24  
Complete Zap Between the  
Electrodes of Fig. 23

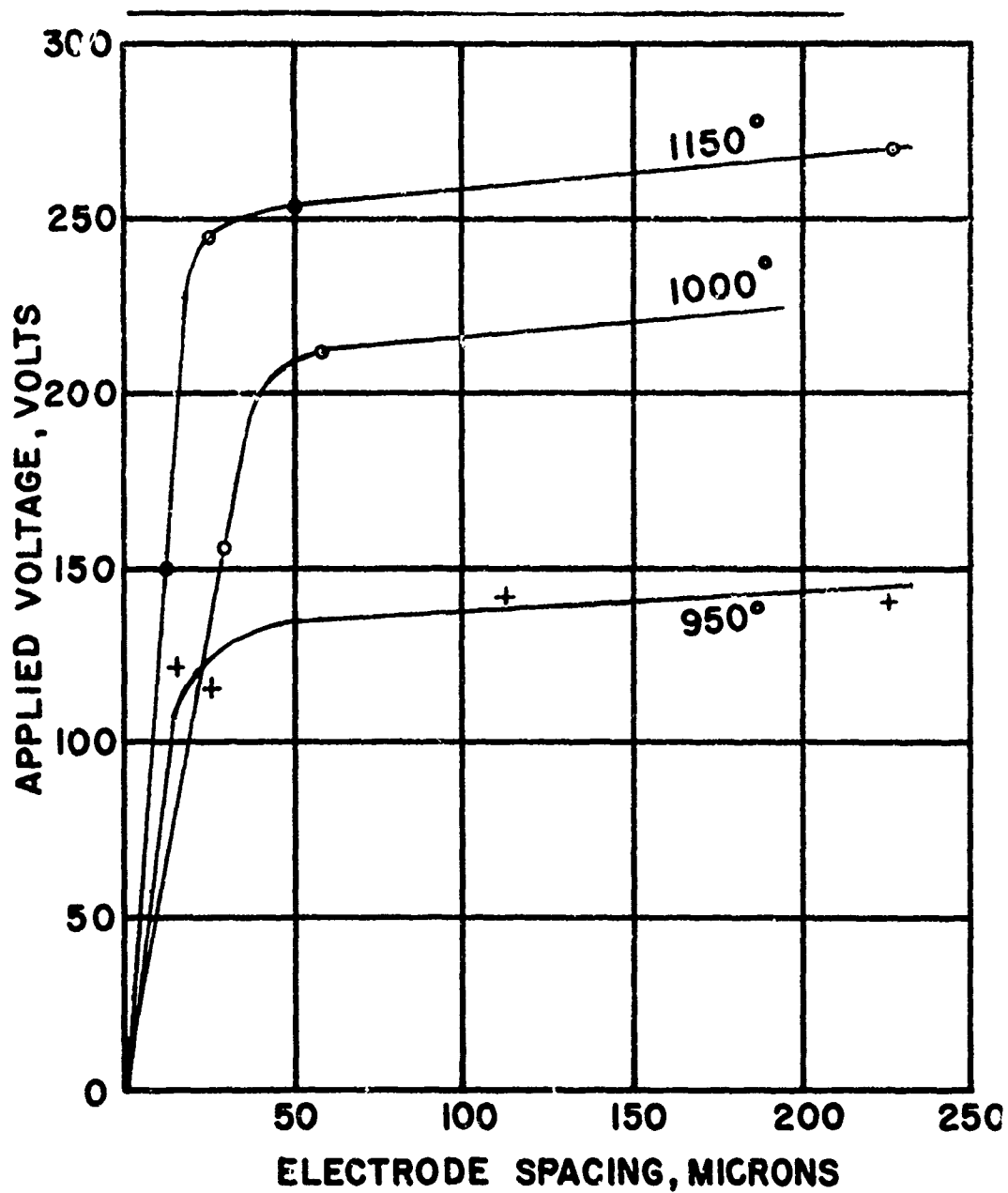


Figure 25  
Variation in Breakdown Voltage  
With Electrode Separation  
For Three Oxidation Temperatures